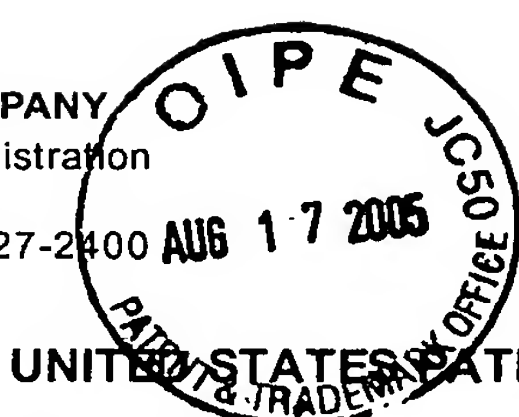


HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400



08-18-05

PATENT APPLICATION

ATTORNEY DOCKET NO. 100111235-1

IFW41

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): S. Brandon Keller, et al.

Confirmation No.: 2834

Application No.: 10/647,608

Examiner: Vuthe Siek

Filing Date: Aug. 25, 2003

Group Art Unit: 2825

Title: SYSTEM AND METHOD FOR DETERMINING UNMATCHED DESIGN ELEMENTS IN A
COMPUTER-AUTOMATED DESIGN

Mail Stop
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- () Response/Amendment () Petition to extend time to respond
() New fee as calculated below () Supplemental Declaration
() No additional fee
(X) Other: Intv Sum, Supp IDS, Form 1449, 1 Ref, & Post Card (fee \$)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS		MINUS		= 0	X \$50	\$ 0
INDEP. CLAIMS		MINUS		= 0	X \$200	\$ 0
[] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ \$360	\$ 0
EXTENSION FEE	1ST MONTH \$120.00	2ND MONTH \$450.00	3RD MONTH \$1020.00	4TH MONTH \$1590.00		\$ 0
OTHER FEES						\$
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$ 0

Charge \$ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. EV413242222US

Date of Deposit August 17, 2005

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By Melissa Smith

Typed Name: Melissa Smith

Respectfully submitted,

S. Brandon Keller, et al.

By Curtis A. Vock

Curtis A. Vock

Attorney/Agent for Applicant(s)
Reg. No. 38,356

Date: August 17, 2005

Telephone No.: (970) 931-3011



PATENT
Attorney Docket No.: 100111235-1
Express Mail Label No.: EV413242222US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	S. Brandon Keller	Confirmation No.	2834
Serial No.	10/647,608	Group Art Unit:	2825
Filed:	August 25, 2003	Examiner:	SIEK, VUTHE
For:	System And Method For Determining Unmatched Design Elements in a Computer-Automated Design	Attorney Docket No.	100111235-1

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT OF THE SUBSTANCE OF INTERVIEW

Sir:

In accordance with 37 C.F.R. §1.133 and MPEP §713.04, Applicants request this "Statement of the Substance of Interview" be entered into the prosecution record of the above-referenced patent application.

On 28 July 2005, Examiner Vuthe Siek initiated a telephonic interview regarding the status of U.S. Patent Application Serial No. 10/647,608. During the course of the interview, Examiner Siek requested a definition of the language "cumulative value of a design element characteristic" as stated in Claim 1.

Further, Examiner Vuthe Siek also requested that we provide, via Email, an amended paragraph [0001] with the proper serial numbers.

On 28 July 2005, Chalynda Renz forwarded an Email with the following amendment.

[0001] The present document contains material related to the material of copending, cofiled, U.S. patent applications ~~Attorney Docket Number 100111221-1, entitled System And Method For Determining Wire Capacitance For A VLSI Circuit; Attorney Docket Number 100111227-1, entitled System And Method For Determining Applicable~~

~~Configuration Information For Use In Analysis Of A Computer Aided Design; Attorney Docket Number 100111228-1, entitled Systems And Methods Utilizing Fast Analysis Information During Detailed Analysis Of A Circuit Design; Attorney Docket Number 100111230-1, entitled Systems And Methods For Determining Activity Factors Of A Circuit Design; Attorney Docket Number 100111232-1, entitled System And Method For Determining A Highest Level Signal Name In A Hierarchical VLSI Design; Attorney Docket Number 100111233-1, entitled System And Method For Determining Connectivity Of Nets In A Hierarchical Circuit Design; Attorney Docket Number 100111234-1, entitled System And Method Analyzing Design Elements In Computer Aided Design Tools; Attorney Docket Number 100111236-1, entitled Computer Aided Design Systems And Methods With Reduced Memory Utilization; Attorney Docket Number 100111238-1, entitled System And Method For Iteratively Traversing A Hierarchical Circuit Design; Attorney Docket Number 100111257-1, entitled Systems And Methods For Establishing Data Model Consistency Of Computer Aided Design Tools; Attorney Docket Number 100111259-1, entitled Systems And Methods For Identifying Data Sources Associated With A Circuit Design; and Attorney Docket Number 100111260-1, entitled Systems And Methods For Performing Circuit Analysis On A Circuit Design, U.S. Patent Application Number 10/647,597, entitled System And Method For Determining Wire Capacitance For A VLSI Circuit; U.S. Patent Application Number 10/647,595, entitled System And Method For Determining Applicable Configuration Information For Use In Analysis Of A Computer Aided Design; U.S. Patent Application Number 10/647,687, entitled Systems And Methods Utilizing Fast Analysis Information During Detailed Analysis Of A Circuit Design; U.S. Patent Application Number 10/647,594, entitled Systems And Methods For Determining Activity Factors Of A Circuit Design; U.S. Patent Application Number 10/647,768, entitled System And Method For Determining A Highest Level Signal Name In A Hierarchical VLSI Design; U.S. Patent Application Number 10/647,606, entitled System And Method For Determining Connectivity Of Nets In A Hierarchical Circuit Design; U.S. Patent Application Number 10/647,596, entitled System And Method Analyzing Design Elements In Computer Aided Design Tools; U.S. Patent Application Number 10/647,598, entitled Computer Aided Design Systems And Methods With Reduced Memory Utilization; U.S. Patent Application Number 10/647,688, entitled System And Method For Iteratively Traversing A Hierarchical Circuit Design; U.S. Patent Application Number 10/647,769, entitled Systems And Methods For Establishing Data~~

Model Consistency Of Computer Aided Design Tools; U.S. Patent Application Number 10/647,607, entitled Systems And Methods For Identifying Data Sources Associated With A Circuit Design; and U.S. Patent Application Number 10/647,605, entitled Systems And Methods For Performing Circuit Analysis On A Circuit Design, the disclosures of which are hereby incorporated herein by reference.

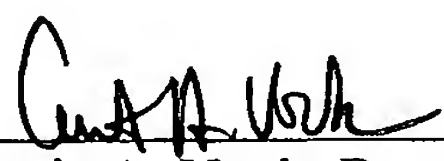
On 29 July 2005, in a telephonic message to Examiner Siek, Curtis Vock provided support for defining "cumulative value of a design element characteristic" as based on the specification and referred to the following segments of the specification:

In paragraph [0007]: "A design element family is a set of two or more design elements, each of which has at least one common electrical or physical characteristic. For example, a P-type MOSFET and an N-type MOSFET may be considered as two members of a design element family. Both types of MOSFETS have common characteristics, such as MOSFET widths (explained below)"

In paragraph [0008]: "In the present system, processor 102 is configured for determining the difference between a cumulative value of a predetermined characteristic of unmatched first type of design elements connected to a given node."

In paragraph [0011]: "The FET width data is part of the circuit information that exists in the data model that represents the circuit, and current density data is provided by a technology file for the process in which the chip is to be constructed. At step 225, this source current value is stored cumulatively (i.e., as a total current value)"

Respectfully submitted,

By: 
Curtis A. Vock, Reg. No. 38,356
LATHROP & GAGE L.C.
4845 Pearl East Circle, Suite 302
Boulder, CO 80301
Telephone: (720) 931-3011
Facsimile: (720) 931-3001